E28J60

ENCJ28J60 INTERNET MODULE

• An SPI interface that serves as a communication channel between the host controller and the ENC28J60.
• Equips control registers for controlling and monitoring the ENC28J60.
• A dual port RAM buffer for received and transmitted data packets.
• An arbiter to control the access to the RAM buffer when requests are made from DMA, transmit and receive blocks.
• The bus interface that interprets data and commands received via the SPI interface.
• The MAC (Medium Access Control) module that implements the IEEE 802.3 compliant MAC logic.
• The PHY (Physical Layer) module that encodes and decodes the analog data that is present on the twisted-pair interface.